REMARKS

Claims 1-24 were pending in this application. By way of this amendment and reply to the Office Action mailed February 19, 2002, "withdrawn from consideration" claims 5, 10, 17 and 24 have been canceled. Therefore, claims 1-4, 6-9, 11-16 and 18-23 are presently pending for further consideration. Applicants reserve the right to prosecute the non-elected claims 5, 10, 17 and 24 in a divisional application, if so desired.

As an initial matter, it is respectfully requested that the Examiner consider the reference submitted with an Information Disclosure Statement (IDS) filed on January 17, 2002, by returning to applicants' representative an initialed copy of the PTO-1449 formed submitted with the IDS.

In the Office Action, the drawings were objected to for the reasons set forth in numbered section 2 of the Office Action. By way of a separate letter submitted herewith, Applicants propose to amend Figure 2 to provide a reference number and lead line for element 123a discussed in the specification, as well as to correct a minor error found in that figure.

In the Office Action, the Abstract was objected to because it was too long. A new Abstract is being submitted herewith, which is within the acceptable word length for Abstracts.

In the Office Action, claims 1-4, 6-9, 11-16 and 18-23 were rejected under 35 U.S.C. § 113(a) as being unpatentable over U.S. Patent No. 6,251,721 to Kanazawa et al. This rejection is traversed for the reasons given below.

It is noted that Kanazawa et al. has a U.S. application filing date of April 7, 2000. Therefore, by the filing of a verified translation of the priority document for this application, Applicants have effectively removed the Kanazawa et al. reference as prior art (the effective filing date of the priority document is December 24, 1999).

Since there are no other objections or rejections raised in the Office Action, Applicants believe that the present application is now in condition for allowance, and an early indication of allowance is earnestly solicited.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

June 4, 2002
Date

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning on page 2, line 21 and ending on page 3, line 10:

Transistor elements 111, 112 have respective source regions 111b, 112b and respective drain regions 111c, 112c formed by introducing an impurity into semiconductor substrate 101 by way of ion implantation. The gaps between source regions 111b, 112b and drain regions 111c, 112c function as respective gate regions 111a, 112a. In cell array region 102, a pair of adjacent transistor elements 111 sharing source region 111b make up memory cell 110. A plurality of memory cells are arranged in a substantially zigzag pattern (see Fig. 2). In peripheral circuit region 103, transistor elements 112 are arranged as desired to form peripheral circuits, though not shown. As a whole, transistor elements 112 in peripheral circuit region 103 are arranged at a density [loner] lower than transistor elements 111 in cell array region 102.

Mark d-Up ABSTRACT OF THE DISCLOSURE

[To manufacture a] A semiconductor device manufacturing proc ss for forming a semiconductor device having a high density region and a low density [regions] region of transistor elements [on a single semiconductor substrate], includes forming a gate oxide film and gate electrodes [are formed] on a semiconductor substrate surface. [of the semiconductor substrate, and oxide films are] Then, a first nitride film is uniformly formed on the gate electrodes[.], and only the low-density region of the semiconductor device is etched. Then, a second nitride film is uniformly formed, and then an interlayer insulating film is formed. [Voids are eliminated by annealing the assembly in water vapor.] The high-density region is self-aligned using the first nitride film as an etch stopper to form contact holes in the interlayer insulating film, and contact electrodes are formed in the contact holes. [Finally, the] The assembly is then annealed by a forming [a] gas to recover an interfacial layer. [Since the second nitride film is positioned on the surface of the semiconductor substrate in the low-density region, an impurity is prevented from being diffused from the interlayer insulating film into the semiconductor substrate and the semiconductor substrate is prevented from being oxidized when the assembly is annealed in water vapor. The second nitride film does not prevent the forming gas from being diffused.]